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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,359	12/14/2001	Michael Joachim Wolf	Q67426	1154

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EXAMINER

JONES, PRENELL P

ART UNIT	PAPER NUMBER
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2616

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/014,359

Applicant(s)

WOLF ET AL.

Examiner

Prenell P. Jones

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2, 10, 14, 18 and 21-23 is/are allowed.
- 6) ☒ Claim(s) 1, 15-17, 19, 20 is/are rejected.
- 7) ☒ Claim(s) 3-9, 11 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 12 of response, that the cited prior art fails to teach or suggest phase matching between 2 delayed clock signals and having 2 internal clocks, whereas a second internal clock signal is adjusted to the phase of the first delayed internal clock signal.

### ***Double Patenting***

1. The nonstatutory double patenting rejection is based on a judicially created doctrine 12 grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 13 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 28 of U.S. Patent No. 6,816,818. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 13 of the present application merely broadens the scope of the claims 28 of the Patent by eliminating the elements and their functions of the claims. It has been held that the omission an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

The difference between claim 13 of the current application and claim 28 of the patent is that claim 28 of the patent includes receiving at least one external clock signal at receiver, a master synchronization signal for synchronization of the output signal of receiver module with the at least one external clock signal, synchronizing the output signal of the at least one receiver module with the at least one regenerated clock signal selected as the master synchronization signal. Although claim 13 of current application describes a computer medium for storing code to execute program code which is a subset of the described methods in claim 28 of the patent, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a computer medium that implements the subset of process/method associated with the claimed method of claim 28 for the purpose of further implementing internal redundancy communication process in a computer environment.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 15-17, 19 and 20 rejected under 35 U.S.C. 102(b) as being anticipated by Hamamoto et al (US Pat 5,987,619).

Regarding claims 1, 15-17, 19 and 20, Hamamoto discloses a phase compensation circuit that includes a first and second delay circuit along with associated internal clocks (FCLK and BCKL), wherein signals are eventually outputted and a clock signal generation circuit that receives clock signals, and delay circuits that receive internal first/second clock signals, delay first internal clock and delay second internal clock, (Abstract, Fig. 7-9, col. 2, line 21-54, col. 5, line 7 thru col. 6, line 47), and adjusting one delayed internal clock to match another delayed internal clock, resulting in the matching internal clock signals, and a first and second clock signals are external clock signals (Fig. 7, 8, 9, 10 & 11)

***Allowable Subject Matter***

1. Claims 2, 10, 14, 18 and 21-23 are allowed over prior art.
2. Claims 3-9, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Although the combined cited art discloses phase compensation associated in a telecommunication environment wherein utilization of a first/second delay unit along with corresponding first/second clock signals and associated delay time, and adjusting the phase, they fail to teach or suggest with respect to claims 3 and 4, first delay time corresponds to a maximum expected phase difference and/or maximum expected propagation time difference between at least one first clock signal and the second clock signal, with respect to claim 5, selecting one of the at least one first delayed clock signal and the second delayed clock signal and optionally one of the at least first clock signal and the second clock signal, where the respective selected, at least one first delayed clock signal or second delayed clock signal serves to synchronize the compensation module, with respect to claim 8, when first delayed clock signal is selected instead of the second delayed clock signal, the delayed first clock signal present at an output end of the first delay means is adapted by adjusting, with respect to claim 9, the first or second start value is performed only upon attainment of a predetermined first deviation tolerance value, while the converse applies upon the attainment of a second deviation tolerance value which is smaller than the first deviation tolerance value, with respect to claims 10 and 11, phase adjustment changes the second delay time of second delay means in dynamic step sizes, a respective step size being modified as a function of the respective phase difference, with respect to claim 14, a SDH transmission network that includes a compensation module for clock signals in the network with SDH, with respect to claim 18, code executed by control means on a console of a network device for a transmission with a SDH.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones 

November 6, 2005

  
CHI PHAM  
SUPERVISORY PATENT EXAMINER 11/9/05